74. IMPLEMENTATION OF MULTIBAND FLEXIBLE DIVIDER WITH SINGLE PHASE CLOCK

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With the increasing demand for low cost and high integration of building blocks of wireless transceiver, the performance of low-power is a great concern for radio-frequency integrated circuit (RFIC) designers. The frequency synthesizer commonly used based on phase-locked loop (PLL) is an important building block of the transceiver. The main role of carrier generation for the down-conversion/up-conversion operations performed by frequency synthesizer, is a major block of a wireless transceiver because it operates at high frequency and consumes a very large amount of the total power consumption. The performance in power consumption and channel selection of frequency synthesizer are limited by the most important building block, frequency divider. The objective of this project work is to design the most critical block for the frequency synthesizer, which is the frequency divider with low power consumption. A dynamic logic multiband flexible divider with wideband multimodulus prescalar 32/33/47/48, for Zigbee and IEEE 802.15.4 applications is implemented based on pulse-swallow topology which uses the ultra-low power 2/3 prescaler, and D flip-flops for the Program counter and Swallow counter.

Keywords— Radio-frequency integrated circuit ,Frequency synthesizer, Phase locked loop, Wideband multimodulus prescaler,Pulse swallow topology.

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