60. DESIGN AND IMPLEMENTATION OF TRUNCATED MULTIPLIER IN FIR FILTER

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Low-cost finite impulse response (FIR) designs are presented using the concept of faithfully rounded truncated multiplier. This multiplier design is usually considered where the maximum absolute error is no more than 1 unit of least position. And also this truncated multipliers offer significant improvement in area, delay and power. The proposed method jointly consider the deletion, reduction, truncation and rounding of partial product bits in order to minimize the number of full adders and half adders during tree reduction. In addition, the truncated multiplier design also has smaller delay due to the smaller bit width in the final carry-propagate adder. In previous papers truncation error is reduced by adding error compensation circuits in fixed width multiplier to get a precised output. But here, there is no need of error compensation circuits and the final output will be precised. The proposed filter using truncatedmultiplier will be designed using VerilogHDL and synthesis using ISE Simulator (ISIM) and simulate it using MODELSIM ALTERA 6.4a (Quartus II 9.2i).It achieves best area and power result when compared with previous FIR design approaches.

KEYWORDS: low power and area truncated multiplier, DSP, VLSI design, FIR filter
Design, partial products.

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