46. DESIGN OF LOW LEAKAGE STANDARD CELLS USING GATE LENGTH BIASING IN CADENCE VIRTUOSO AND ALU USING POWER GATING SLEEP TRANSISTOR TECHNIQUE IN SOC ENCOUNTER

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The leakage current, power and area have become import parameters in circuit designing as the technology is scaling.Leakage power has become one of the most critical design concernsfor the system level chip designer. While lowered supplies and hence lowered threshold voltage) and aggressive clock gating can achieve dynamic power reduction, these techniques increase the leakage power and, therefore, causes its share of total power to increase. The basic gates such as inverter, NAND, and NOR are important elements in digital circuits.Gate length biasing is a method to optimize the design by varying the gate length so as to decrease power dissipation. In the current technology, the leakage power is the major contributor to the total power consumption . Power gating and clock gating are technique which are used to reduce the leakage power by switching off the unused transistors and clock using sleep transistor technique

keywords— standard cell , gate length , power dissipation, sleep transistor , power gating , clock gating , leakage power.

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