321. A RECONFIGURABLE PARALLEL PIPELINING VLSI ARCHITECTURE FORLOW LATENCY 3-D DWT LIFTING

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Optimizing image compression is a craft balance between compression and PSNR ratio. Numerous 2D wavelet mechanisms are introduced throughout the literature and reached its superiority over various other compression schemes. This paper work presents a novel methodology of 3D wavelet for lifting for video and color band compression, in this method the spatial and frequency relation between video frames will be considered for achieving better compression and reconstruction PSNR ratios. A parallel processing VLSI architecture is demanded due to the implications of complex and delay inducing equations, whereas the design constraint of a VLSI parallel architecture required to have a fixed number of picture groups for processing i.e. for jthlevel of the video frame, j number of processing units are required to operate in parallel. This work proposes to optimize this limitation by designing a dynamically reconfigurable 3D wavelet lifting architecture.

Keywords—Wavelet, Lifting Scheme, VLSI, FPGA

ISBN 978-81-904760-6-5