320. REVERSE CONVERTER DESIGN VIA PARALLEL-PREFIX ADDERS: NOVEL COMPONENTS, METHODOLOGY AND IMPLEMENTATIONS

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In this brief, the implementation of residue number system reverse converters based on well-known regular and modular parallel prefix adders is analyzed. The VLSI implementation results show a significant delay reduction and area × time2 improvements, all this at the cost of higher power consumption, which is the main reason preventing the use of parallel-prefix adders to achieve high-speed reverse converters in nowadays systems. Hence, to solve the high power consumption problem, novel specific hybrid parallel-prefix-based adder components that provide better tradeoff between delay and power consumption are herein presented to design reverse converters. A methodology is also described to design reverse converters based on different kinds of prefix adders.

Keywords - RNS, Parallel prefix adder, Reverse converter, VLSI

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