307. IMPLEMENTATION OF COARSE GRAINED DYNAMICALLY RECONFIGURABLE ARCHITECTURE FOR DSP APPLICATIONS

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Coarse grained dynamically reconfigurable architecture offers 16 bit or 32 bit operation which can be re-fused based on DSP applications and performs the same operation using single element by hardware reuse optimization. The complex multiplication is implemented using single multiplier which is used in implementation of FIR, FFT, DCT, its inverse transforms and ALU operations and achieve hardware resource minimization.

Keywords—Coarse gtained; reconfigurable;

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