301. MEMORY-HIERARCHICAL AND MODE-ADAPTIVE HEVC INTRA PREDICTION ARCHITECTURE FOR QUAD FULL HD VIDEO DECODING

J.Subramaniabharathi
ME(Applied electronics)
Meenakshi College of Engineering
Chennai

This paper presents a high-throughput and area efficient VLSI architecture for intra prediction in the emerging high efficiency video coding standard. Three design techniques are proposed to address the complexity systematically: a hierarchical memory deployment that stores neighboring samples in of static RAM (SRAM) instead of gates of registers and increases throughput by processing reference samples in registers a mode-adaptive scheduling scheme for all prediction units, which provides at least 2 samples/cycle throughput while using low-throughput SRAM and can achieve2.46 samples/cycle on the average based on the experimental results; and resource sharing for multipliers and the read out circuits of reference sample registers, which can save 2.5-k gates. These techniques can efficiently reduce area by 40% but induce more power because of additional signal transitions

Keywords—Wavelet, Lifting Scheme, VLSI, FPGA

ISBN 978-81-904760-6-5