265. LOW POWER DESIGN OF LOGIC GATES USING DUAL MODE LOGIC

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The power consumption is one of the important considerations in VLSI digital design due to advancement in technology and the extension of mobile applications. The low-power Dual Mode Logic (DML) family is a logic family designed to operate in the sub-threshold region. This logic family can be switched between static and dynamic modes of operation according to system requirements. The unique feature of the DML provides the option to control system performance and thus support applications in which a flexible workload is required. In the static mode of operation, the dual mode logic gates have very low-power dissipation with moderate performance and in the dynamic mode of operation they have better performance. In this paper, the conventional logic gates are compared to the DML Type A and Type B gates and the results are analysed in terms of power consumption. This can be analysed from a comparison of DML NAND and DML NOR gates to conventional NAND and NOR gates respectively. The simulation results are obtained using the Tanner EDA Tools.

Keywords— Dual Mode Logic (DML), low power dissipation, static mode, dynamic mode.

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