258. DESIGN AND SIMULATION OF LOW POWER WIDE FAN-IN GATES

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This paper deals about the wide fan-in gates design with low leakage and less area overhead. The growth of technology leads to shrink of component size and reduce area of chip. So, it is important to reduce the power dissipation for the present technology scaling. In these cases, overcoming the leakage current is a great challenge. According to International Technology Roadmap for Semiconductor (ITRS) projects, the leakage power is one of the dominant dissipation of total power consumption. To overcome the leakage, different methods are proposed in previous approaches. We proposed "Leakage Resistant Domino" which is a novel structure for OR gate designto reduce the leakage current. Unlike the previous approaches, it improves the noise immunity without degradation in the performance. The proposed design is validated by 130nm technology for power and frequency comparisons.

Keywords - OR gate; Domino logic; Leakage current; Power dissipation; Current mirror.

ISBN 978-81-904760-6-5