230. FPGA IMPLEMENTATION OF FLOATING POINT MULTIPLIER USING VEDIC MATHEMATICS

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Floating Point (FP) Multiplication is widely used in more complex scientific and signal processing computations. Multiplication is one of the most commonly used arithmetic operations which is widely used in DSP, microprocessor, data processing applications etc.. In these computations a high speed floating point multiplier based on Vedic mathematics is implemented on vertex-5 FPGA. Vedic mathematics is one of the ancient methodologies in Indian mathematics which was introduced in 20th century which is based on 16 sutras (formulas) and 13 sub-sutras. The most efficient techniques under Vedic mathematics is Nikhliam sutra and Urdhva Triyagbhyam sutra In this Paper the sub-modules are coded in Verilog HDL synthesis and simulated it using the Xilinx ISE tool which are aimed on FPGA. The main aim of the multiplication is to increase the speed by reducing the delay.

Keywords: Vedic Mathematics, Floating Point Multiplier, FPGA and Urdhva Triyakbhyam

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