227. AN AREA EFFICIENT CARRY BASED CARRY SELECT ADDER

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In electronic applications, adders are used extensively. Carry Select Adder (CSLA) is the fastest adders to perform arithmetic functions in many data processing processors. In designing adigital circuit, area, delay and power is a major problem. Carry select adder is taken to minimize any of those parameters. Conventional based CSLA and Binary to excess one code converter (BEC) based CSLA is the basis technique which is already present, but it not that much efficient. To overcome those drawbacks, the proposed system called Carry based Carry Select Adder is designed. The area can be reduced with slight increase in the delay when compared to BEC based CSLA. It can be synthesized and simulated in Xilinx ISE tool at Verilog language.

Index terms– Binary to excess one converter, Carry select adder, Conventional logic gates, Ripple carry adder, MUX.

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