224. VLSI IMPLEMENTATION OF RECONFIGURABLE FFT PROCESSOR USING VEDIC MATHEMATICS

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Fast Fourier transform has been used in wide range of applications such as digital signal processing and wireless communications. In this we present a implementation of reconfigurable FFT processor using single path delay feedback architecture. To eliminate the use of read only memory's (ROM'S), these are used to store the twiddle factors. To achieve the ROM-less FFT processor the proposed architecture applies the bit parallel multipliers and reconfigurable complex multipliers, thus consuming less power. The proposed architecture, Reconfigurable FFT processor based on Vedic mathematics is designed, simulated and implemented using VIRTEX-5 FPGA. Urdhva Triyakbhyam algorithm is an ancient Vedic mathematic sutra, which is used to achieve the high performance. This reconfigurable DIF-FFT is having the high speed and small area as compared with other conventional DIF-FFT.

Key words – Bit parallel multiplier, Complex multiplier, FFT, Vedic mathematics

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