182. VLSI IMPLEMENTATION OF AREA AND POWER EFFICIENT DELAYED LMS ADAPTIVE FILTER

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This paper presents the implementation of delayed least mean square (DLMS) adaptive filter with an efficient architecture. A novel partial product generator and optimized balanced pipelining across the time consuming combinational blocks of the structure helps to achieve lower adaptation delay and area delay. From synthesis results, the proposed design is found to have less area delay product (ADP) and less energy delay product (EDP) than the existing systolic structures, for various filter lengths. The optimization of the design across the time consuming combinational blocks reduces the number of pipeline delays along with the area, sampling period and energy consumption. Fixed point implementation scheme is proposed in thearchitecture. In terms of power delay product (PDP) and energy delay product (EDP), the proposed design is more efficient than the existing systolic structures.
Index Terms- Adaptive filter, adder tree optimization, balanced pipelining , least mean square algorithm , fixed-point arithmetic.

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