179. DESIGN AND SYNTHESIS OF EFFECTIVE HIGH SPEED AND LOW POWER CARRY SELECT ADDER

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In this paper an Effective Carry Select Adder (CSLA) design solution is provided for Very Large Scale Integration (VLSI) designers. The design is used to improve the problem of carry propagation delay and also to reduce the power and area consumption used to generate the carry and sum. The existing designs uses full adder (FA) using ripple carry adder (RCA) unit and more amounts of gates to compute sum and carry which result in more area, longer propagation delay and large power consumption and power dissipation. The proposed work aims to reducing the area, power and design complexity by using Effective – Area – Power – square-root (SQRT) CSLA architecture. The new logic operation is proposed for the CSLA to improve its performance. The proposed CSLA design is compared with the existing CSLA designs in terms of area and power.

Keywords - Area-efficient, low power, CSLA, BEC.

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